Claims

What is claimed is:

1. A video graphics and audio processing circuit comprising:

a graphics processing circuit;

an audio processing circuit;

a local bus operably coupled to transceive data to and from the graphics processing circuit and the audio processing circuit; and

a bus arbitrator operably coupled to the local bus, the graphics processing circuit, and the audio processing circuit, wherein the bus arbitrator interprets incoming data and provides the incoming data to the audio graphics processing circuit or to the video graphics processing circuit, and wherein the bus arbitrator arbitrates outputting data on the bus from the graphics processing circuit and the audio processing circuit.

2. The video graphics and audio processing circuit of claim 1, wherein the bus arbitrator comprises an address decoder operably coupled to receive an address via the bus, to route received data to the audio processing circuit when the address identifies the audio processing circuit and to route received data to the graphics processing circuit when the address identifies the graphics processing circuit.

3. The video graphics and audio processing circuit of claim 2, wherein the address decoder comprises control circuitry that generates an output data control signal based on the address and a data command signal.

4. The video graphics and audio processing circuit of claim 3, wherein the bus arbitrator further comprises an output data switch operably coupled to output data to the bus from the audio processing circuit or the graphics processing circuit based on the output data control signal.

5. The video graphics and audio processing circuit of claim 4, wherein the output data switch comprises an audio buffer that stores audio output data generated by the audio processing circuit, an graphics buffer that stores graphics output data generated by the graphics processing circuit, and a multiplexor operably coupled to the audio buffer and the graphics buffer, wherein the multiplexor outputs the audio output data or the graphics output data based on the output data control signal.

6. A method for bus arbitration between an audio processing circuit and a graphics processing circuit, the method comprises the steps of:

a) receiving at least one address;

b) determining whether the at least one address identifies at least one of: the audio processing circuit and the graphics processing circuit; and

c) when the at last one address identifies both the audio processing circuit and the graphics processing circuit, arbitrating access to a local bus between the audio processing circuit and the graphics processing circuit.

7. The method of claim 6, wherein step (a) further comprises receiving an associated command for each of the at least one address.

8. The method of claim 7 further comprises enabling the audio processing circuit to receive incoming data via the local bus when at least one address identifies the audio processing circuit and when the associated command is for inputting data.

9. The method of claim 7 further comprises enabling the graphics processing circuit to receive incoming data via the local bus when at least one address identifies the graphics processing circuit and when the associated command is for inputting data.

10. The method of claim 7 further comprises providing the audio processing circuit access to the local bus when the at least one address identifies the audio processing circuit and the associated command is for outputting data.

11. The method of claim 7 further comprises providing the graphics processing circuit access to the local bus when the at least one address identifies the graphics processing circuit and the associated command is for outputting data.

12. The method of claim 7, wherein the at least one address comprises a plurality of addresses.

13. The method of claim 12 further comprises intermixing the audio processing circuit's access to the local bus with the graphics processing circuit's access to the local bus based on the plurality of addresses and the associated command.

14. A video graphics and audio processing circuit comprising:

a processing unit; and

memory operably coupled to the processing unit, wherein the memory stores programming instructions that, when read by the processing unit, cause the processing unit to receive at least one address and an associated data command for each of the at least one address; audio process the associated data command when the at least one address identifies audio processing, and graphics process the associated data comment when the at least one address identifies graphics processing.

15. The video graphics and audio processing circuit of claim 14, wherein the memory further comprises programming instructions that cause the processing unit to determine whether the associated data command is for inputting data or outputting data.

16. The video graphics and audio processing circuit of claim 15, wherein the memory further comprises programming instructions that cause the processing unit to intermix outputting audio data and graphics data when the at least one address includes a plurality of addresses that identify both the audio processing and graphics processing.

17. An arbitrator that arbitrates access to a local bus between graphics processing circuit and an audio processing, the arbitrator comprising:

a processing unit; and

memory operably coupled to the processing unit, wherein the memory stores programming instructions that, when read by the processing unit, cause the processing unit to receive at least one address, determine whether the at least one address identifies at least one of: the audio processing circuit and the graphics processing circuit; and arbitrate access to the local bus between the audio processing circuit and the graphics processing circuit when the at last one address identifies both the audio processing circuit and the graphics processing circuit.

18. The arbitrator of claim 17, wherein the memory further comprises programming instructions that cause the processing unit to receive an associated command for each of the at least one address.

19. The arbitrator of claim 18, wherein the memory further comprises programming instructions that cause the processing unit to enable the audio processing circuit to receive incoming data via the local bus when at least one address identifies the audio processing circuit and when the associated command is for inputting data.

20. The arbitrator of claim 18, wherein the memory further comprises programming instructions that cause the processing unit to enable the graphics processing circuit to receive incoming data via the local bus when at least one address identifies the graphics processing circuit and when the associated command is for inputting data.

21. The arbitrator of claim 18, wherein the memory further comprises programming instructions that cause the processing unit to provide the audio processing circuit access to

the local bus when the at least one address identifies the audio processing circuit and the associated command is for outputting data.

22. The arbitrator of claim 18, wherein the memory further comprises programming instructions that cause the processing unit to provide the graphics processing circuit access to the local bus when the at least one address identifies the graphics processing circuit and the associated command is for outputting data.

23. The arbitrator of claim 18, wherein the at least one address comprises a plurality of addresses, and wherein the memory further comprises programming instructions that cause the processing unit to intermix the audio processing circuit's access to the local bus with the graphics processing circuit's access to the local bus based on the plurality of addresses and the associated command.